Electromigration Failure in Au and Joule Heating Induced Oxidation in Cu Conductors - Part 1

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Background/Motivation

Electromigration is the mass transport of a metal due to the momentum transfer between conducting electrons and metal atoms. Electromigration was discovered more than 100 years ago and it has been a problem ever since. As device features reduce in Ultra-large-scale integrated circuits, current densities increase with the metallization layer complexity. These issues make understanding Electromigration (EM) induced failure essential to design more reliable circuits.

In this work, electromigration of copper and gold conductors targeted for microinductor System on a Chip (SoC) applications is studied. We intend to use this study to predict:

1. **Maximum current densities that can be used in microinductor interconnects.**
2. **Expected device life-time under use conditions.**
3. **Identify failure mechanisms in SoC metallization structures.**

Device Description

The electromigration test structures were fabricated alongside the microinductors on glass substrates and on a silicon wafers. They consist of planar copper or gold patterns sandwiched between two ferromagnetic layers, 6.75-μm permalloy (NiFe). Isolation is achieved through an AZ5214 (bottom) and an SO-3 (top) dielectric layer of about 0.5 μm thickness each. The copper is electroplated on a Cr/Au seed layer in SO-3 trenches to a thickness of about 20 μm. In the electromigration test structure, the upper ferromagnetic layer is omitted to allow visual observation of electromigration damage. The size of the electromigration test structure is 4.5 mm by 2.5 mm. The structure contains 24 test lines (1.41 mm long) and one temperature monitor line (left in Fig. 1). The Cu interconnects lines are 3.75um thick.

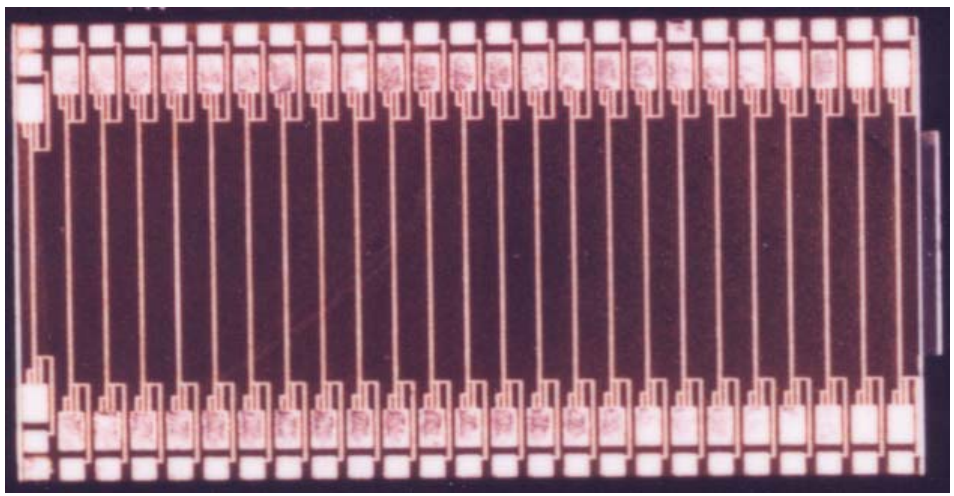
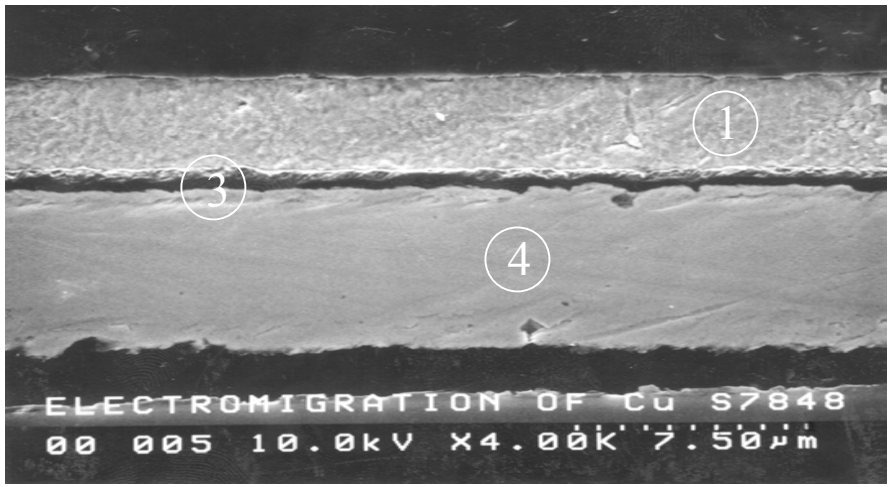
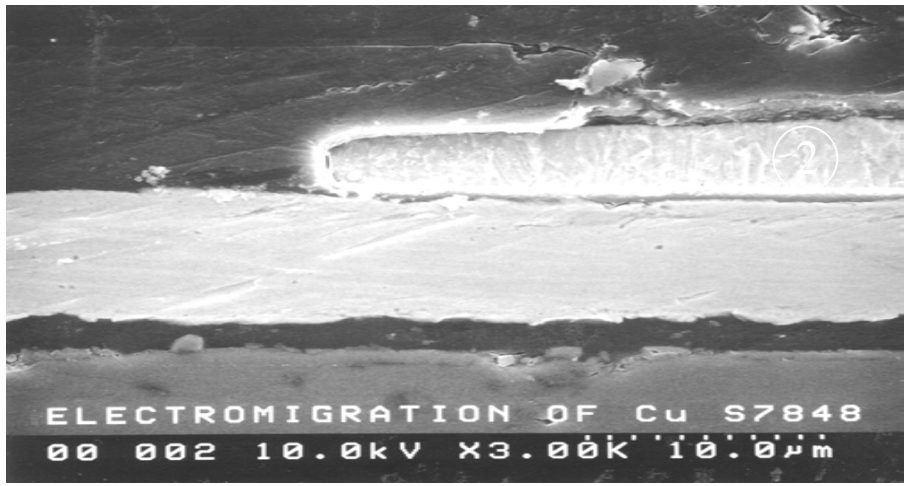


Figure 1. Copper or gold electromigration test structure (Size is 2.5 by 4.5 mm)



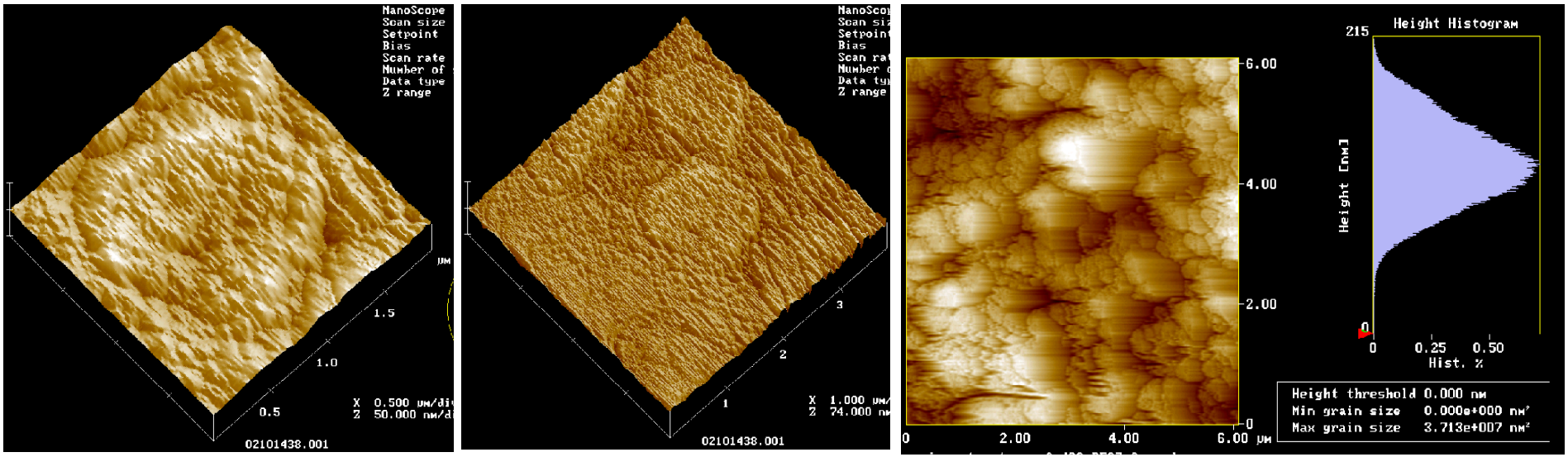


Cross sectional area micrograph of Cu structure; (a) cross section of Cu line; (b) cross section under bonding pad. Standard cross-sectioning techniques using mechanical grinding with light etchings were used to image the structure in cross-section.

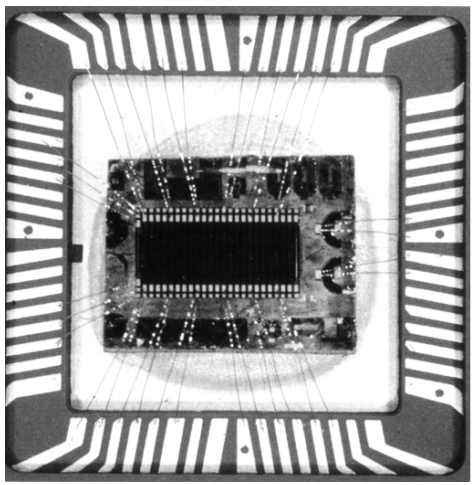
1. Gold or Copper conductor.
2. Gold or Copper bond pad.
3. Dielectric layer between metal (Cu or Au) and NiFe permalloy layer.
4. NiFe permalloy layer.

Microstructure and Morphology

The electromigration structures were analyzed under an Atomic force microscope, where the maximum Cu grain size in the interconnects (bond pads) was found to be about 6-7 μm, the average grain diameter is roughly 1 μm, and the surface roughness ~ 32.5 nm.



(a) And (b) Deflection AFM image in contact mode. (c) shows a lower magnification AFM height image of a larger area which depicts a typical bond pad microstructure in the SoC microinductor metallization structures.

Test set-up:

- **Electromigration structures were mounted wire bonded to a 64 pin package.**
- **Digital acquisition of resistance data vs time at various temperatures was done using two independent calibrated power supplies and digital volt meters.**