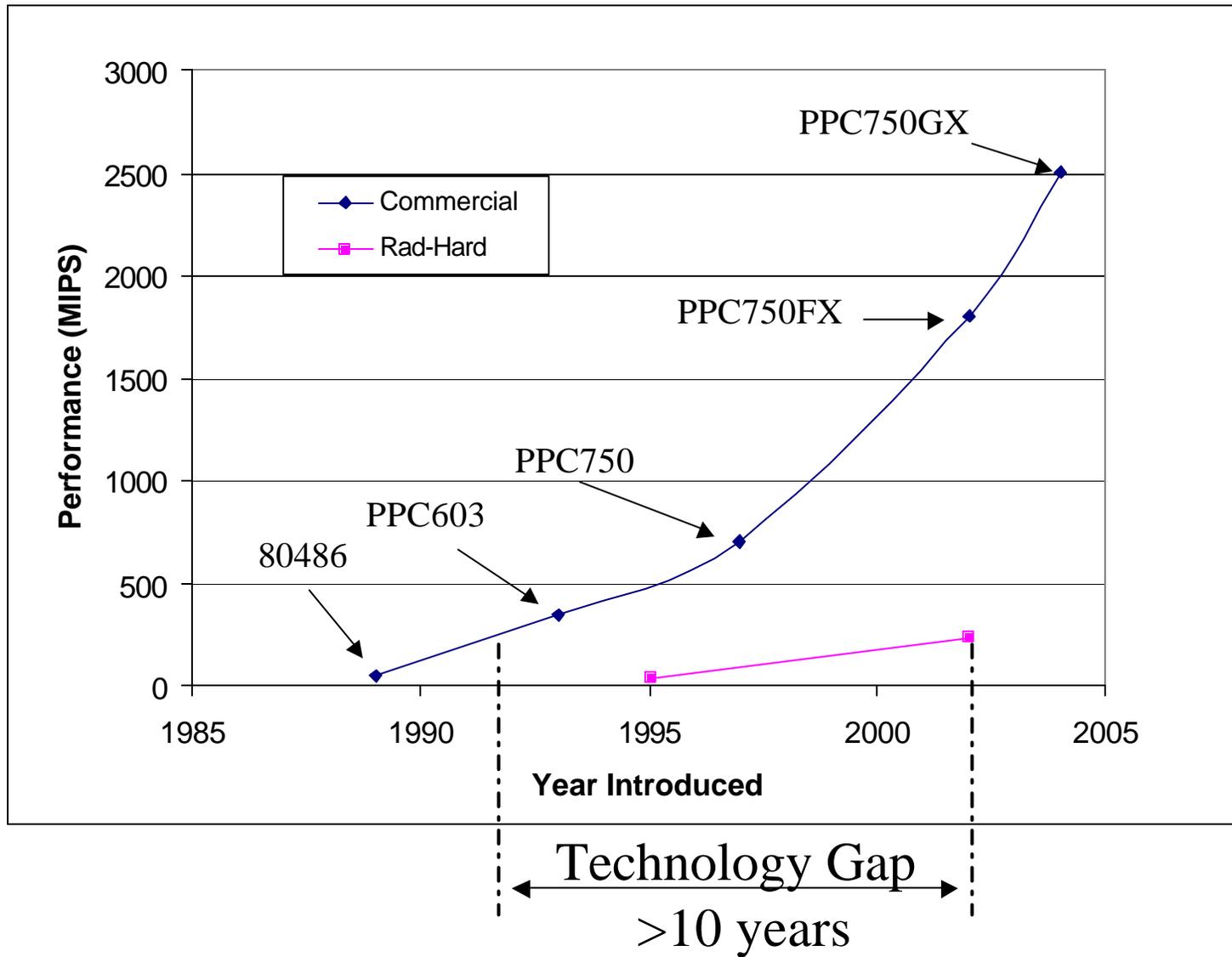

Space Processor Radiation Mitigation and Validation Techniques for an 1800 MIPS Processor Board

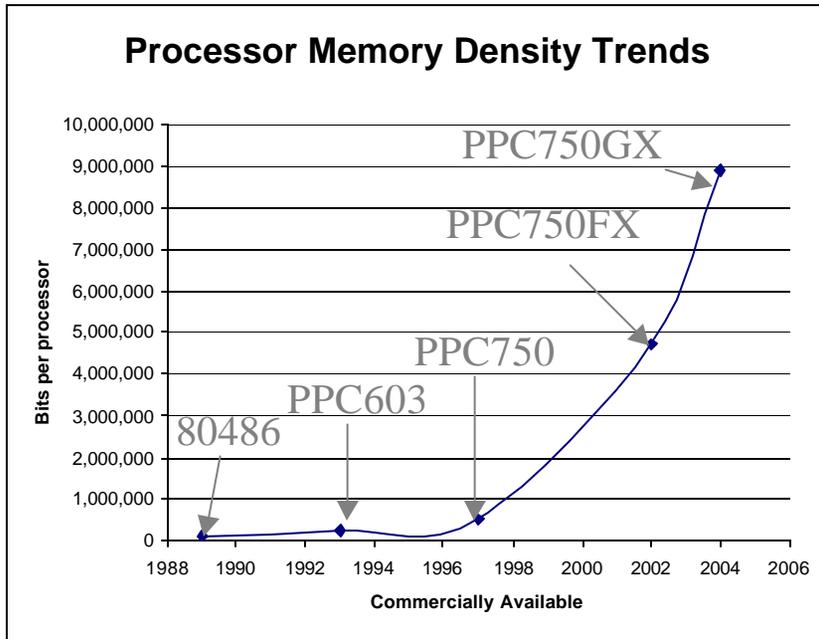
**Robert Hillman, Mark Conrad,
Phil Layton and Chad Thibodeau**
Maxwell Technologies

Gary M. Swift and Farokh Irom
Jet Propulsion Laboratory / California Institute of Technology

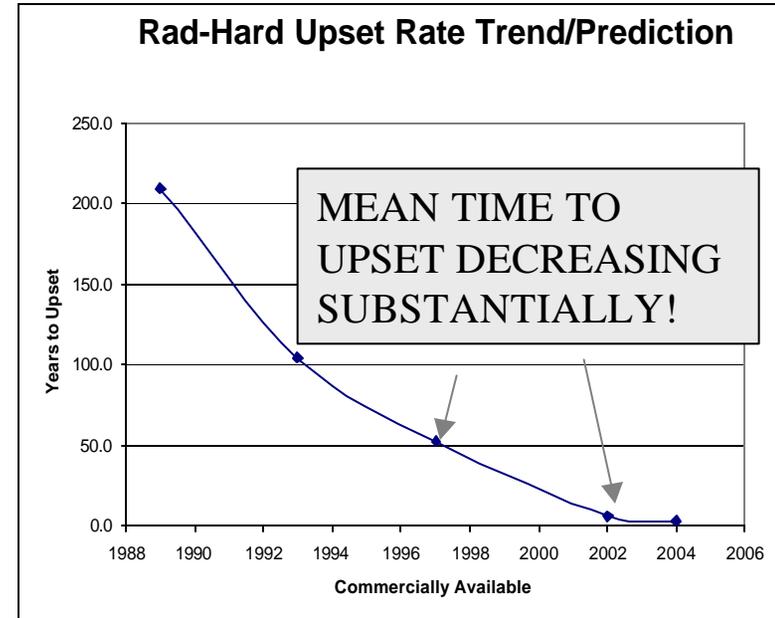
-
- Commercial & Rad-Hard Processor Trends
 - MIPS: Rad-Hard L1 vs. Commercial L1/L2
 - SCS750 Design Strategy
 - Processor & SDRAM Error Correction
 - Development Plan
 - Heavy Ion Test Results (JPL)



Rad-Hard Upset Trend: Less SEU Immunity

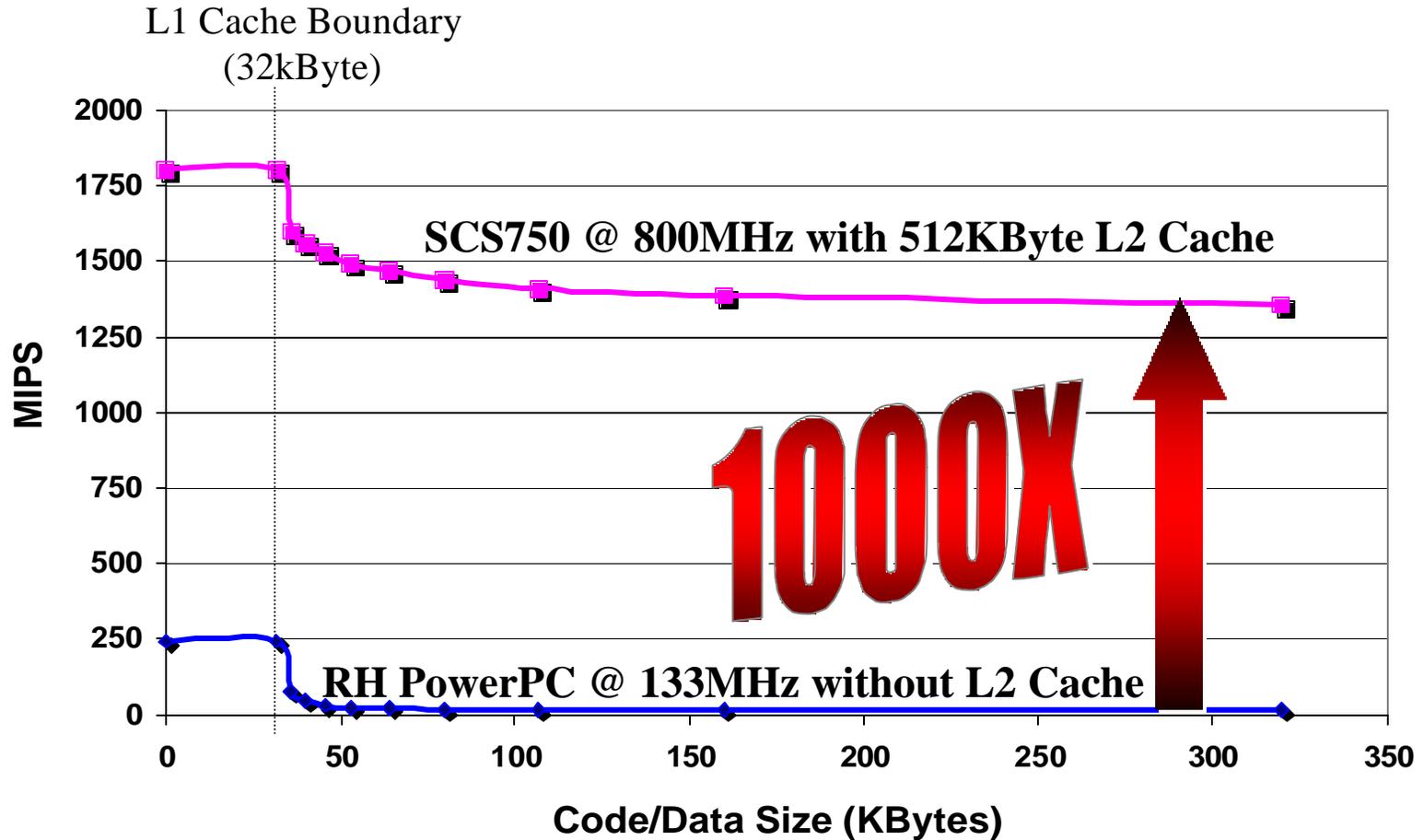


Processor Bits Increasing Exponentially
Dominated by L1 and L2 Cache Sizes



Mean Time to Upset Decreasing Exponentially
Due to Increasing Bits Per Device (Caches)
* Assumes 1E-10 Upsets/bit-day

Error Correction is Needed
Rad-Hard is insufficient with increasing number of bits



**L2 Cache on-chip is Critical
for High Performance**

Commercial Technology

Latest SOI
PowerPC @
800MHz

High Performance
SDRAM

On-Board
Control Logic

Mitigation Technique

TMR/Resynch
& Scrubbing

Double Device
Correct & HW Scrub
(Reed-Solomon)

Actel
RT-AXS
Built-in TMR

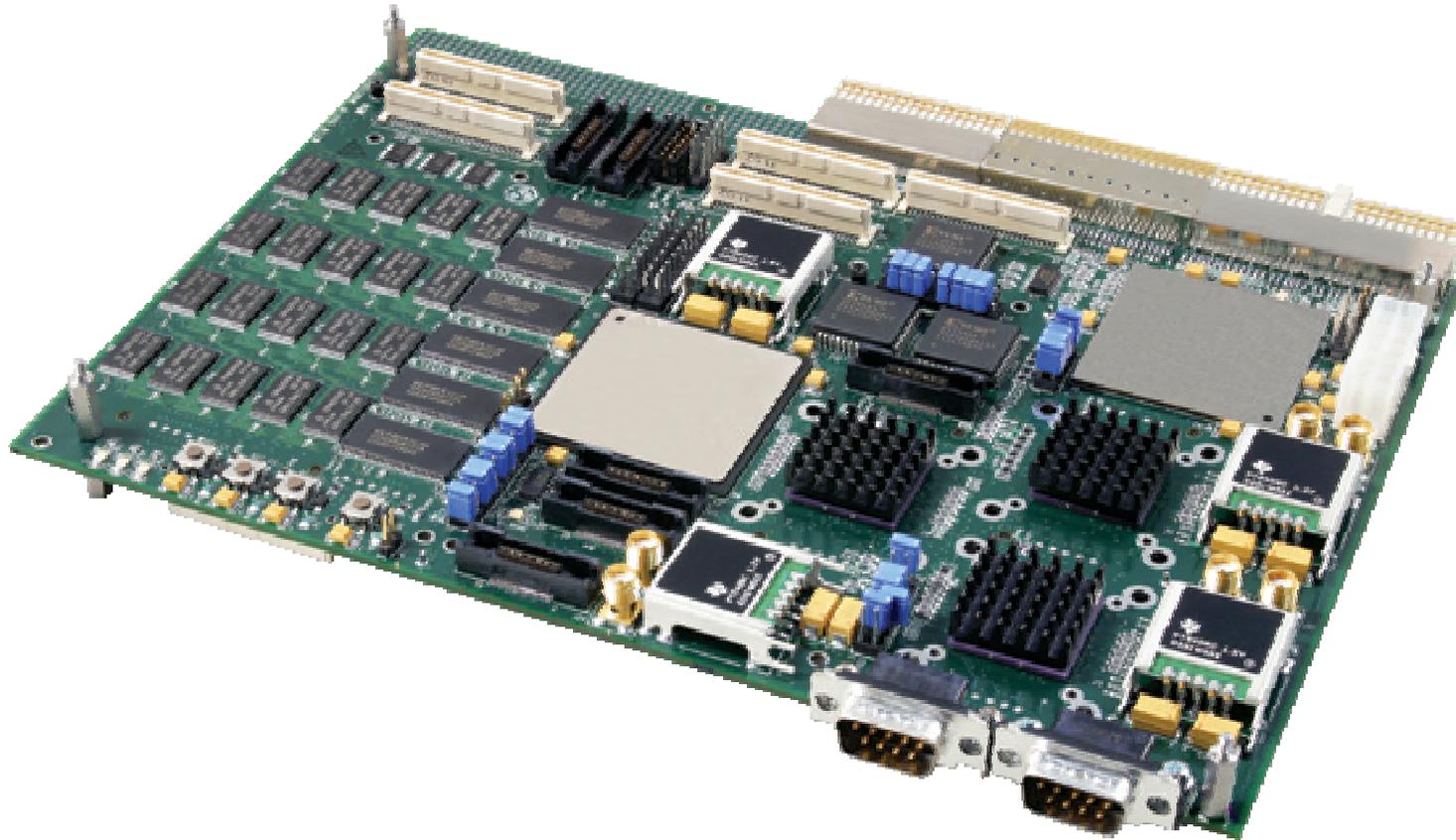
Result

SCS750
1 Uncorrected
Error > 300 Years

~ 1 Upset Per Day
Unacceptable

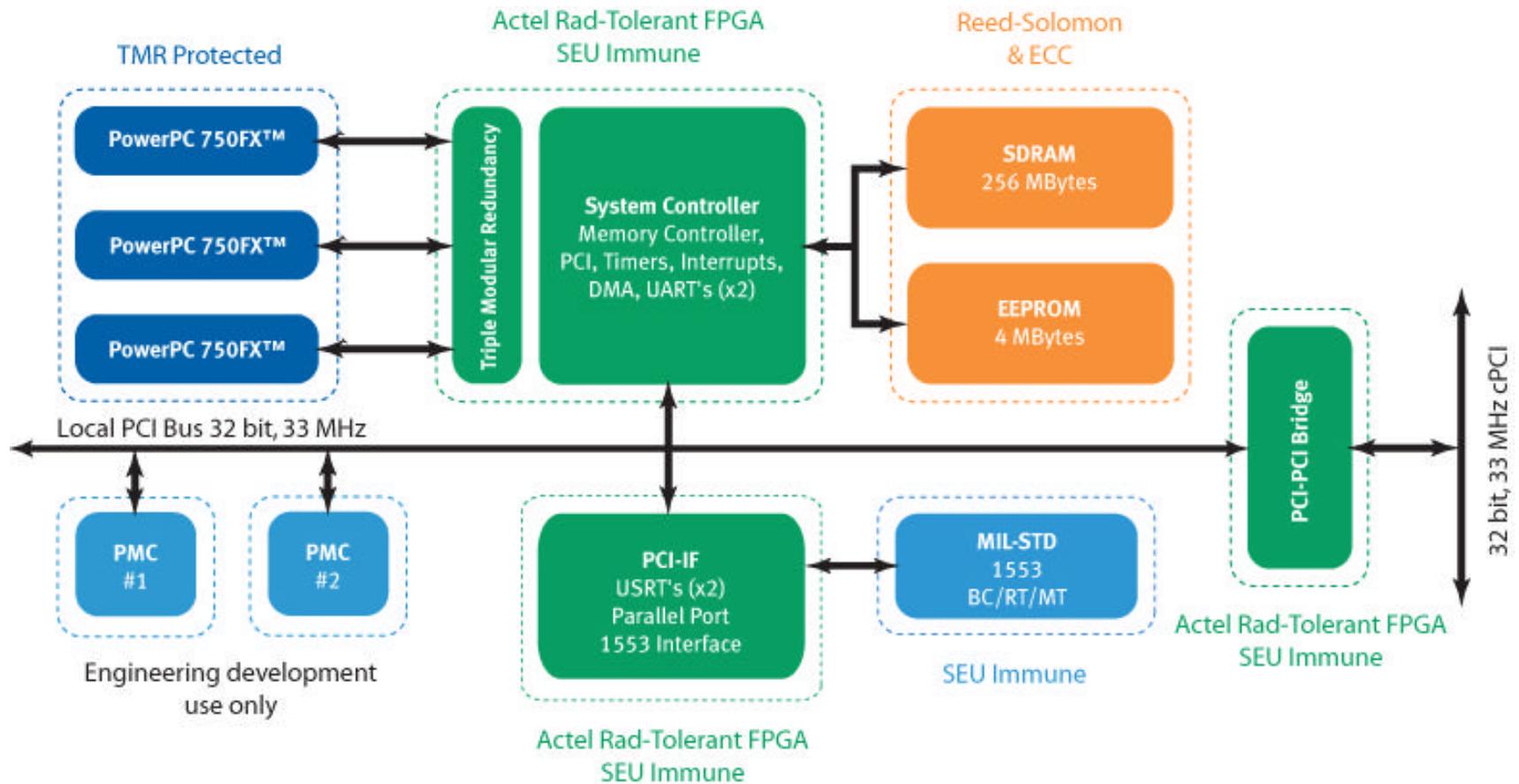
Better Upset
Immunity Than
Rad-Hard SBC's!





Prototype Engineering Module (PEM) – Early Dev. Platform

**FM Boards will be conduction cooled with class S or
equivalent components**



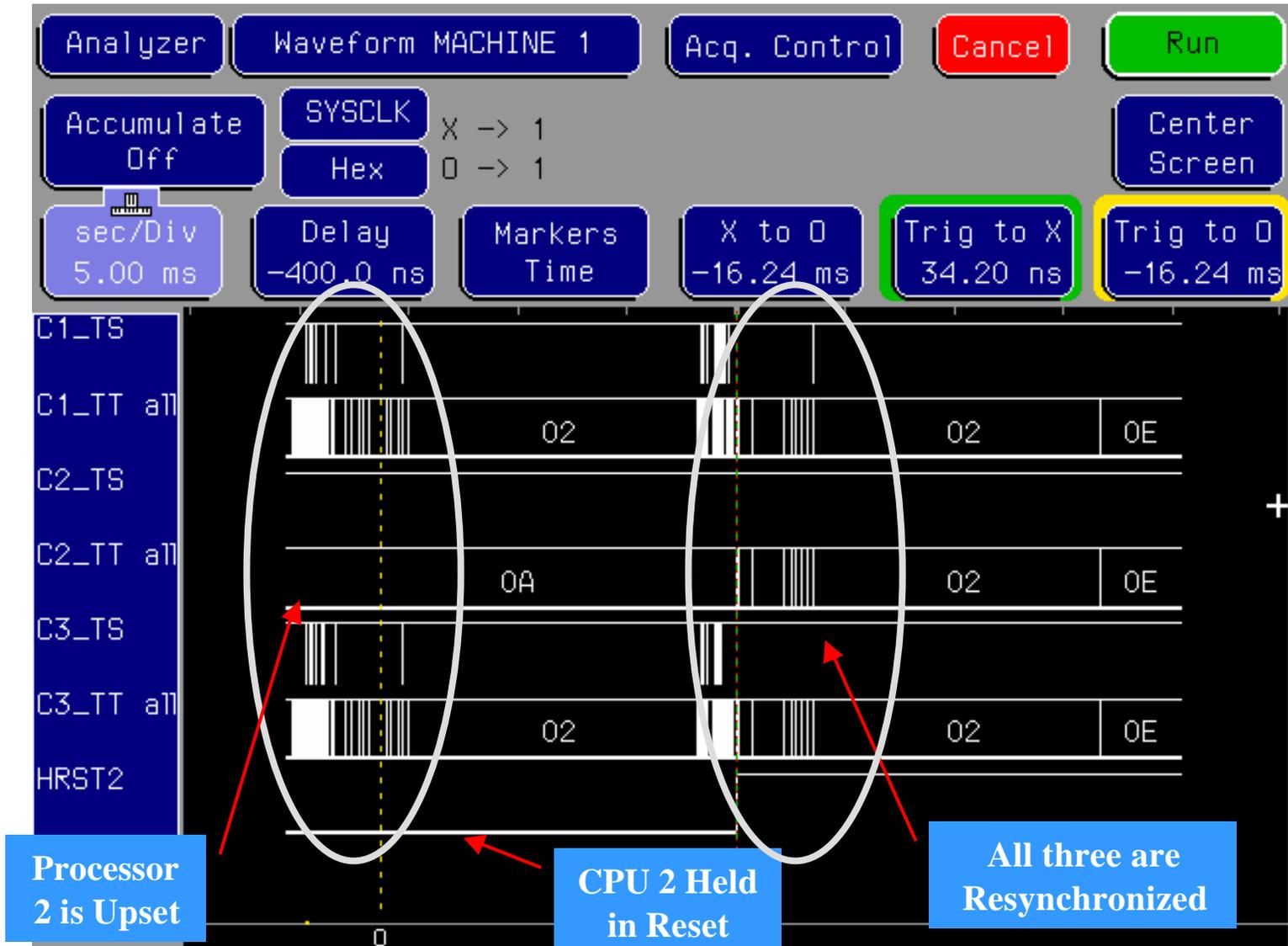
- Entire board designed from the ground up to have the highest upset immunity and highest performance
- All components Latch-Up Immune
 - Component Screening
- Effective SEU rate (entire board!) $< 1E-5$ /board-day
 - One error every 300 years or better!
 - Reed-Solomon, TMR/Scrubbing, component selection
 - Typical Geosynchronous orbit
- Total Dose ≥ 100 KRad
 - Component screening and/or shielding

- 0.13um SOI, Copper interconnect, SiLK
- Extremely low power, runs at 1.2V – 1.5V
- 400MHz, ~ 2Watts each → >900 MIPS
- 800MHz, ~ 4 Watts each → > 1,800 MIPS
- L1 cache 32KB I, 32KB D with parity
- L2 Cache 512KByte on-chip, built-in SEC/DED EDAC
 - L2 cache runs at full processor clock rate
 - Tags are parity protected
- Dual PLL's for on-the fly software control of clock rate
- ★ Future products are drop-in compatible

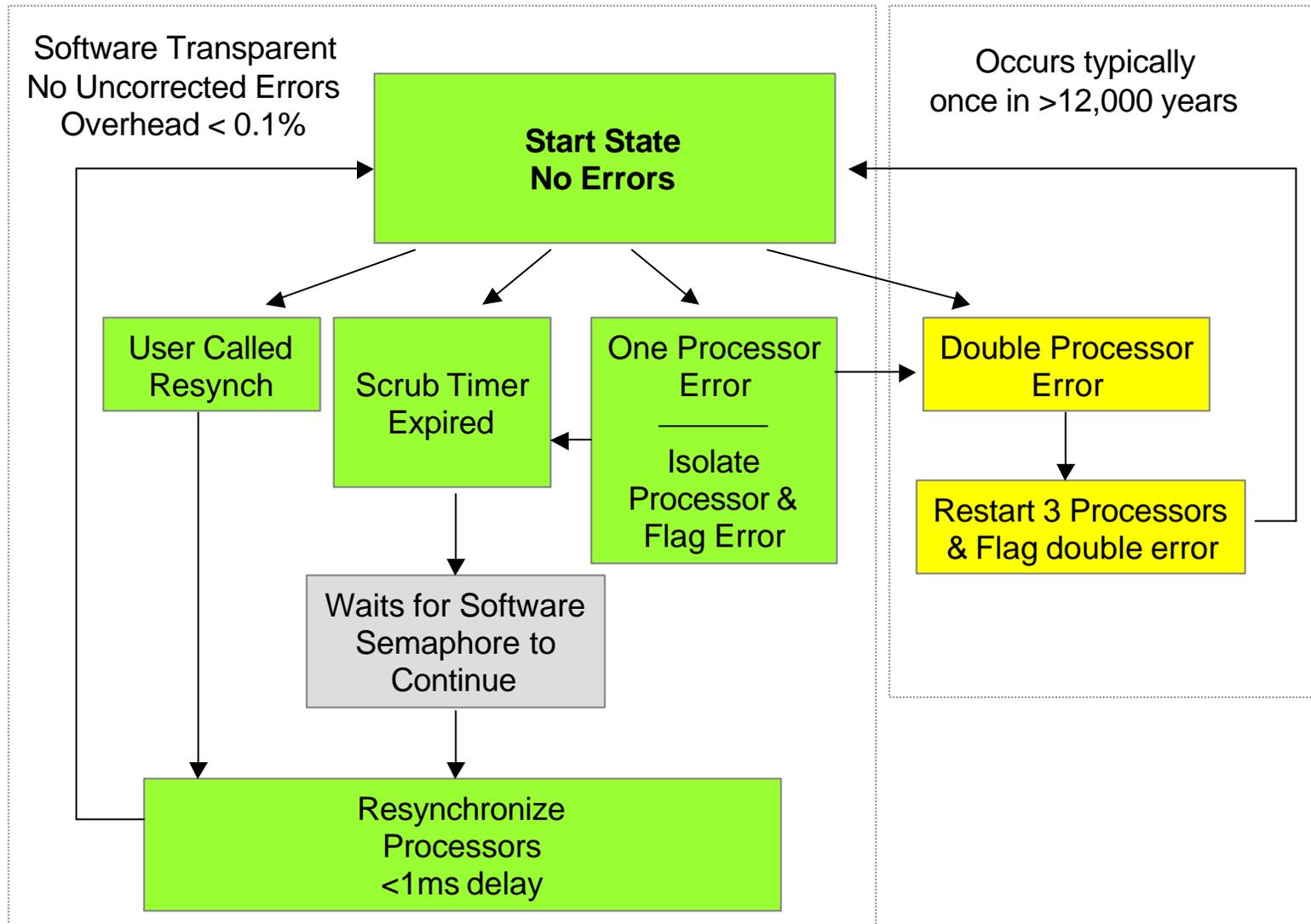
- **Triple Modular Redundant (TMR) Processing**
 - Three processors, each completely isolated
 - No delay in voting (voting and controller all on one chip!)
- **Detection**
 - Single processor error: Flags & Isolates Processor
 - Detection of double processor error & auto restart
- **Resynchronization & Scrubbing**
 - Saves processor states, Resets, Re-loads processor
 - Proven to correct any single event effect in the processors
 - < 1 ms delay, < 0.3% overhead with 1 second scrub

Transparent to Application Software!

Processor Correction Snapshot



Processor Error Correction Flow



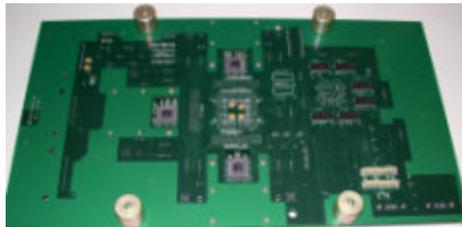
SDRAM Error Correction Comparison

	EDAC Description	Data Bits	Check Bits	Correction / Detection Capabilities	Time to First Failure
Worst  Best	No Error Correction	64	0	None	5 days
	Modified Hamming Code 64/8	64	8	SEC, DED	0.5 years
	Triple Modular Redundancy	64	128	SEC, multi-bit errors/device failures	5 years
	Nibble EDAC 64/16	64	16	Nibble Correct, Double Nibble Detect	24 years
	Reed-Solomon – Implemented on the SCS750	64	32	Double Nibble Correct	12 Million years

Assumptions: 256 Mbyte Memory
Memory Scrub 1 per day

SCS750 has built-in, programmable hardware memory scrubbing (DMA)

Sept 02



Prototype

- Demonstrated
 - *TMR (Voting)*
 - *Error Detection*
 - *Resynchronization*
 - *Radiation Performance*

Xilinx FPGA's for Prototype Development

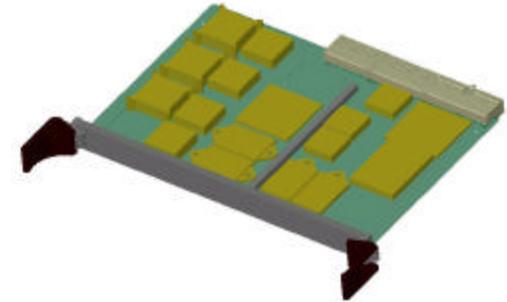
Phase I – July 03

Phase II – Dec 03



SCS750 Proto Engineering

- Software compatible with flight
- Same form factor
- Commercial parts
- Customer development



SCS750 EM – Q2 04

- Engineering boards will use “E” or “I” (Engineering or Industrial Grade)

SCS750 FM – Q4 04

- Flight board
- Fully qualified
- All parts class “S” or equivalent

**Actel Axcellerator,
RT-AX For Flight**

Space Processor Radiation Mitigation and Validation Techniques for an 1800 MIPS Processor Board

Heavy Ion Test Results

Gary M. Swift and Farokh Irom

Jet Propulsion Laboratory / California Institute of Technology

Robert Hillman, Mark Conrad and Phil Layton

Maxwell Technologies

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Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

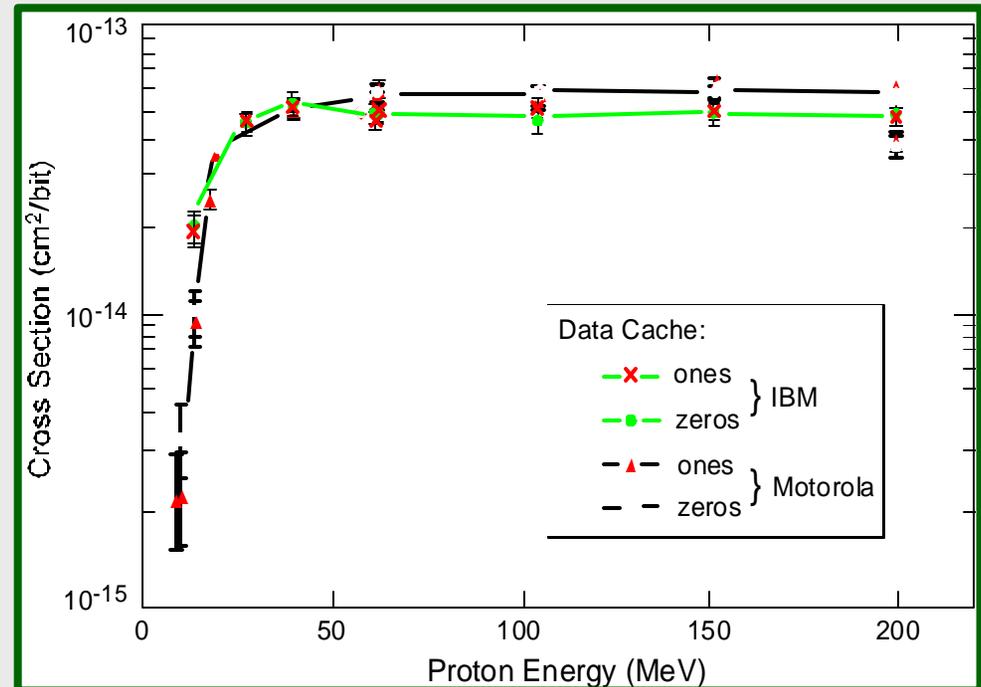
In 2001 at NSREC, we concluded:

From a radiation standpoint, both manufacturers' PowerPC750s are usable for *non-critical* space applications that are like on-board data processing

- Low upset rate
- Very low "hang" rate
 - Occasional reset or re-power needed
 - Upset-aware exception handlers needed

Proton upsets dominate heavy ion rates for environments with proton components, such as:

- Earth Orbit (due to trapped protons)
- Large Flares



Today, we consider:

Can system design add sufficient robustness to upset for *critical* applications?

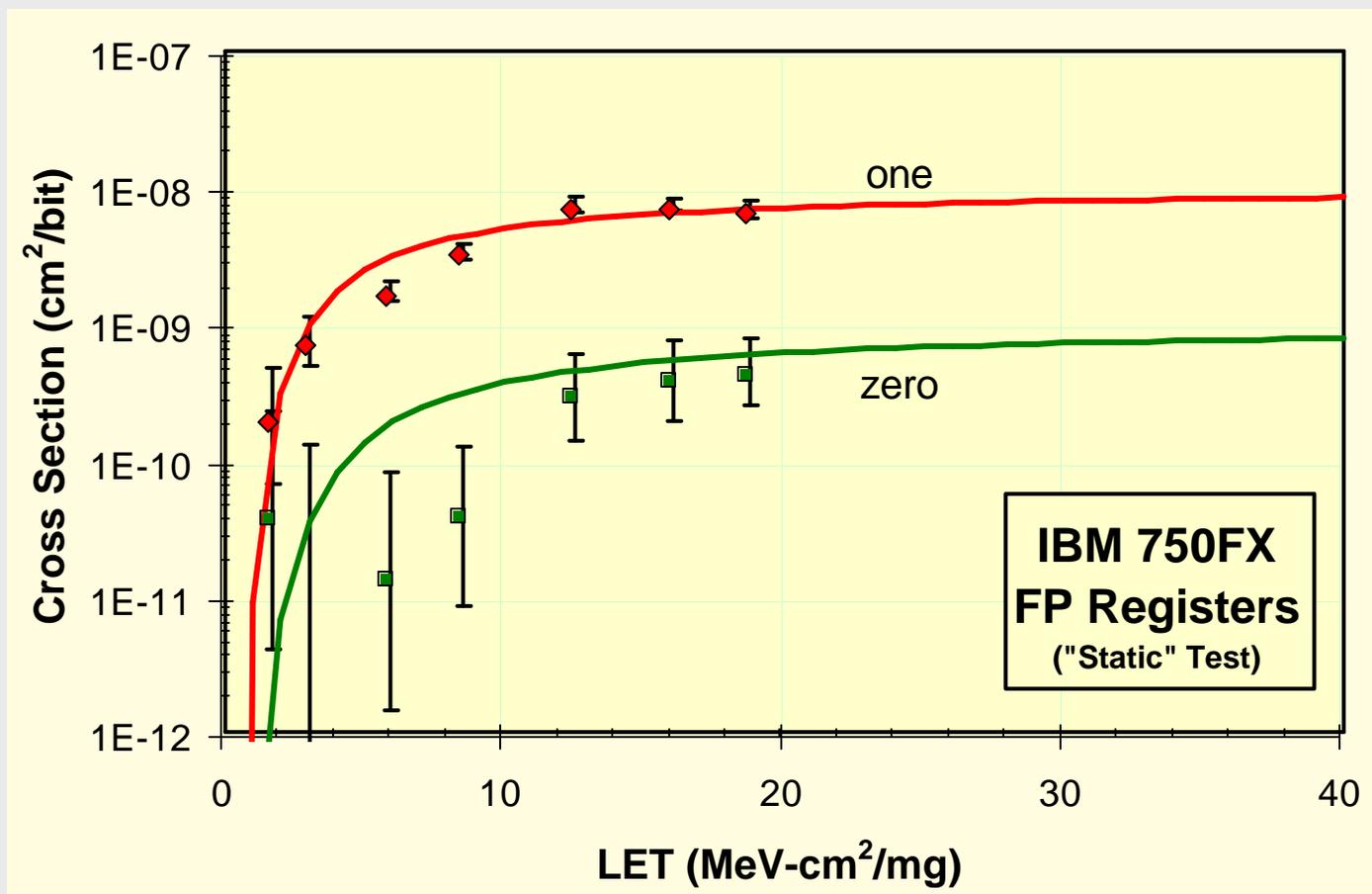
OUTLINE

- Single Processor Results for IBM PPC750 FX
 - Earlier “static” data
 - “Dynamic” test data
- Three Processor Results on Maxwell SCS750 PEM
 - System Mitigation Dependences
 - Flux more important than fluence
 - Linear with scrub rate
 - Re-syncs and Reset Results
- In-flight Upset Rate Comparison

Note: PEM = Prototype Engineering Module

Upset Susceptibility of the IBM PPC 750 FX

From the NSREC 2002 dataset:



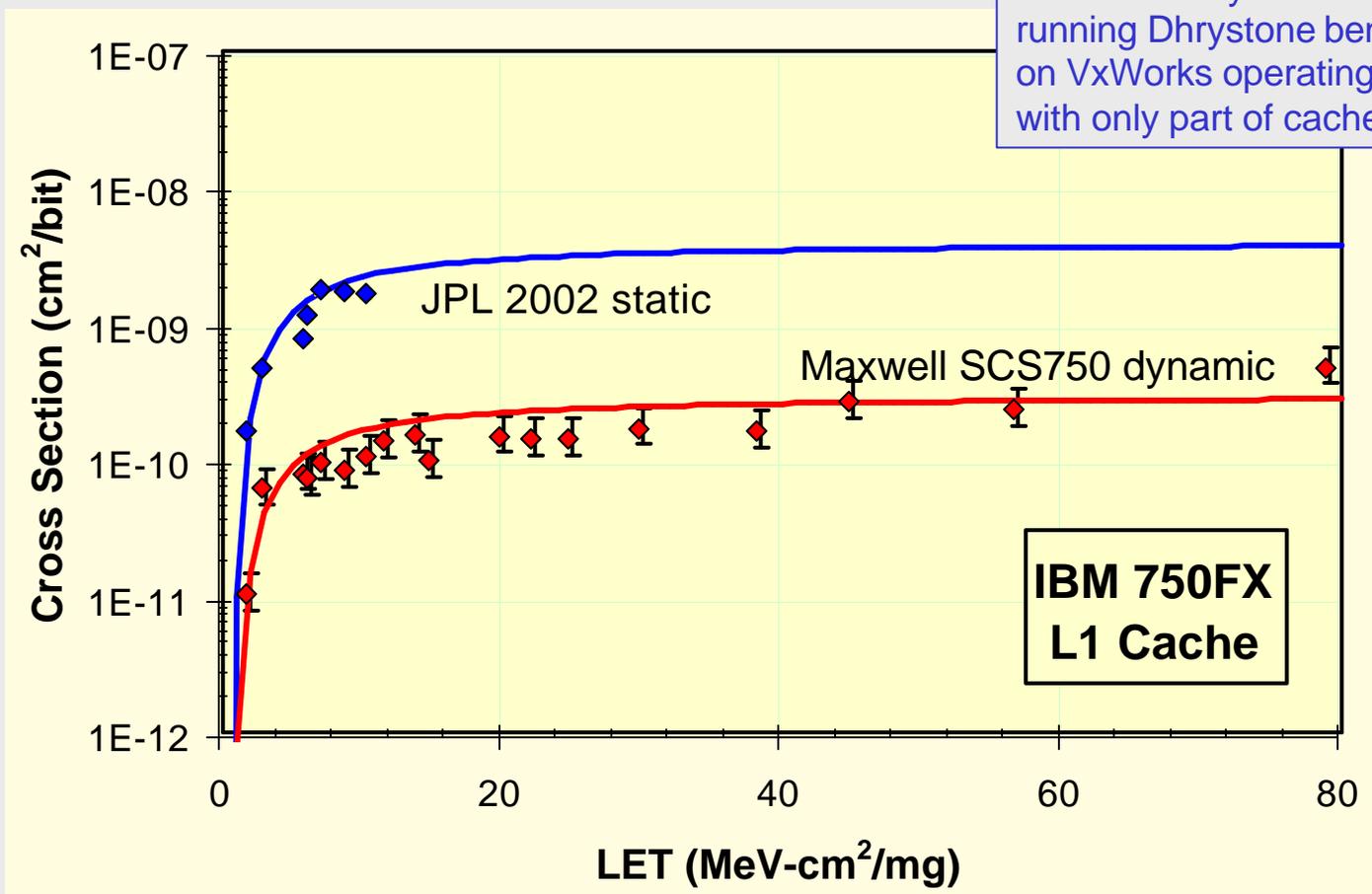
Note: two sigma error bars

Typical Register Results

Upset Susceptibility of the IBM PPC 750 FX

Comparing the new results:

Note: New dynamic test is running Dhrystone benchmark on VxWorks operating system with only part of cache in use.



New test is dynamic (<100% bit duty cycle), so results lower.

Test Comparison

Differences in:

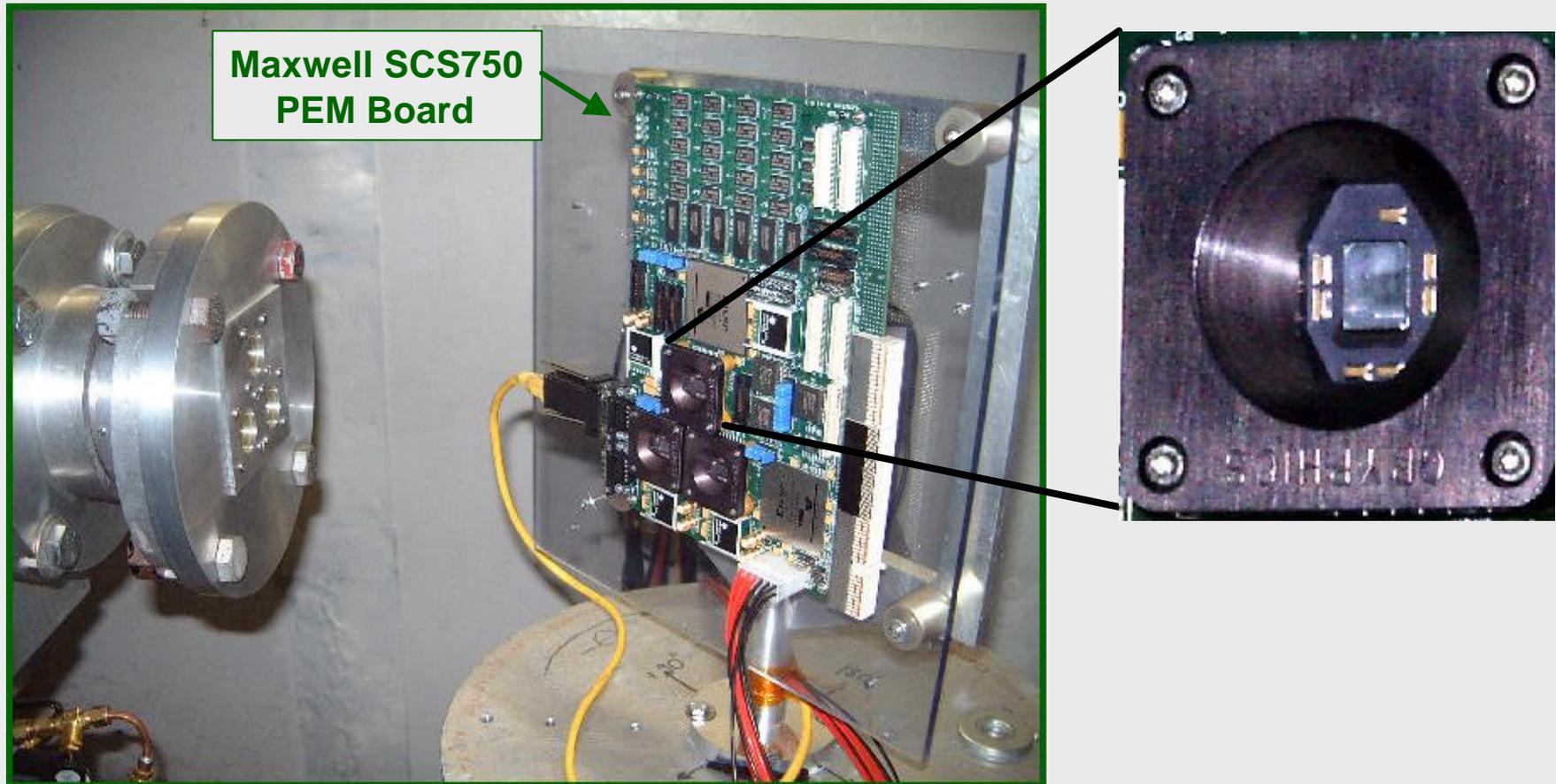
board	-	SCS750 PEM	vs.	Yellowknife
OS	-	VxWorks	vs.	none
program	-	Dhrystone	vs.	do nothing loop
background	-	scrub	vs.	snapshots
speed	-	400 MHz	vs.	500 MHz
die rev	-	DD2.2	vs.	DD1

Most important difference:

“Application” Test vs. “Register” Test

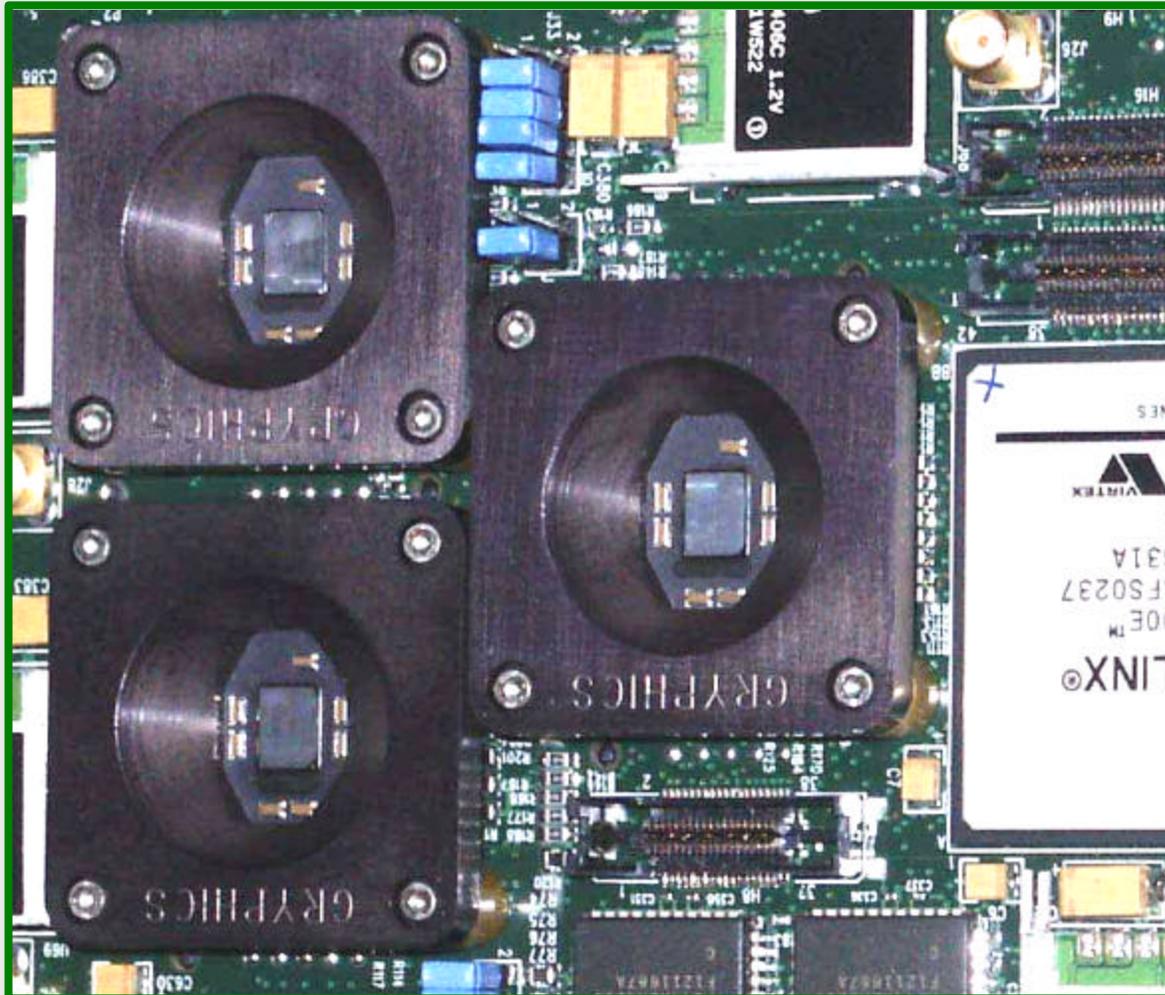
Three Processor Test Setup

At the Texas A&M Cyclotron Facility:



Test Setup – Beam Uniformity

At the Texas A&M Cyclotron Facility:



Upsets by Processor

Run	uP-A	uP-B	uP-C
47.1	67	82	82
47.2	20	20	15
47.3	63	66	62
47.4	22	18	19
47.5	113	157	131
47.6	27	32	23
47.7	45	56	37

Excellent
Uniformity

Maxwell Upset Mitigation

- Regular re-sync “scrubs” single processor upsets
- Upsets in two processors within a scrub window will require *reboot*

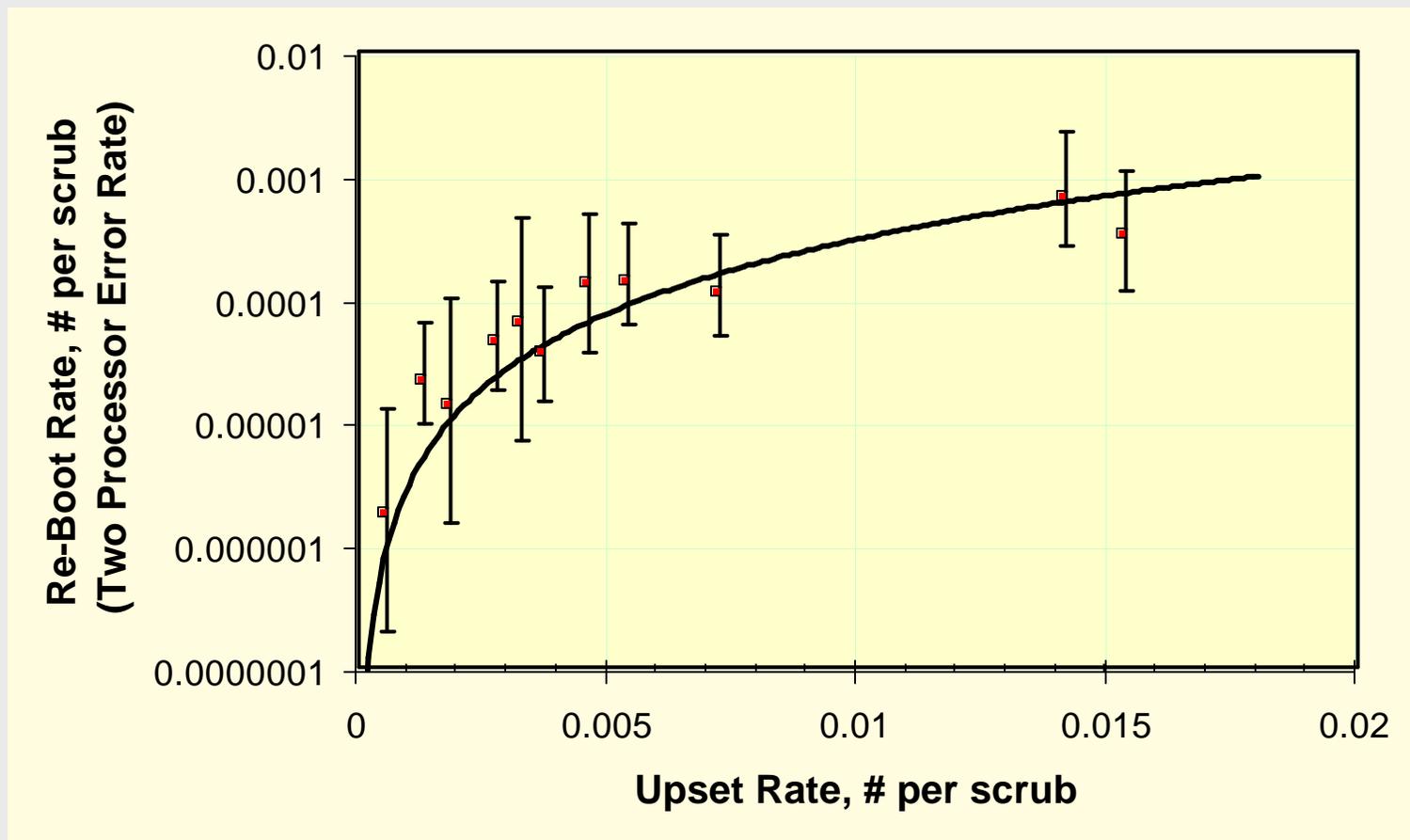
- Equation:

$$\text{Reboot Rate} = 3 \times (\text{Upset Rate})^2 \times \text{Scrub Time}$$

- Rate of resets (double errors) goes as:
 - Upset rate (or flux) squared
 - Proportional to scrub time

SCS750 Triple Processor Results

Reboot rate as a function of upset rate (or flux)



Good correlation with equation

Error Rate Comparison

Environment	750FX Single Processor	Maxwell SCS750 Processors
GCR	34 /yr	1.1E-5 /yr*
DCF heavy ions only	250 /flare	0.22 /flare*
DCF including protons	320 /flare	0.36 /flare*

Notes: For shielding of 100 mil Aluminum-equivalent, and use of **100%** of registers and L1 caches

GCR = **G**alactic **C**osmic **R**ay background at solar minimum

DCF = JPL **D**esign **C**ase **F**lare (at one A.U.)

(similar in size to Oct. '89 and Jan. '72 events)

* Scrub @ 10/sec, performance overhead of < 3%

Error Rate Comparison

	BAE RAD6000 Processor	Maxwell SCS750 Processors	Ratio
GCR	0.2 /yr	1.1E-5 /yr ¹	16,000
DCF	0.6 /flare ²	0.36 /flare ^{1,3}	1.5

NOTES: for shielding of 100 mil Aluminum-equivalent, and use of **100%** of registers and L1 caches

GCR = Galactic Cosmic Ray background at solar minimum

DCF = JPL Design Case Flare (at one A.U.), similar in size to Oct. '89 and Jan. '72 events

¹Scrub @ 10/sec, performance overhead of <3%

²Heavy ions only; according to BAE data, proton susceptibility is minimal

³Including protons at 0.14 /flare

CONCLUSION

- Under heavy-ion irradiation, the SCS750 upset mitigation scheme detected and corrected all single processor errors.
 - This mitigation scheme proved to be *very effective* for the test programs used which are very processor intensive.
 - The performance hit for periodic re-syncing (scrubbing) is small.
- Upon the coincidence of an upset in two processors, the SCS750 successfully recovered with a reboot and reported the double processor error.
 - Coincident errors should be very rare in space.
 - In-beam coincident errors occurred at the expected rates.
- Power cycling was never required for correction.

Commercial processors hardened with the SCS750 architecture can give upset rates comparable to or better than the RAD6000 in space environments.